Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently Amended) ~~A~~ The semiconductor integrated circuit according to claim ~~1,~~ 9 wherein the testing arrangement further ~~comprising~~ comprises an enable input, the enable input being arranged to prevent writing to the memory after writing the selected bit pattern to the memory.

3. (Currently Amended) ~~A~~ The semiconductor integrated circuit according to claim ~~1,~~ 9 wherein the bit pattern for a given address comprises a function of ~~the~~ an address bit sequence, and wherein the data generator is arranged to present the bit pattern at outputs corresponding to address inputs of the memory.

4. (Currently Amended) ~~A~~ The semiconductor integrated circuit according to claim ~~1,~~ 9 wherein the testing arrangement further ~~comprising~~ comprises an arrangement of multiplexers to selectively connect the memory to the combinational logic components of the integrated circuit, or to the data generator.

5. (Currently Amended) ~~A~~ The semiconductor integrated circuit according to claim ~~1,~~ 9 wherein the testing arrangement further ~~comprising~~ comprises an address generator ~~for generating~~ to generate addresses of the memory to which the bit pattern is to be written, the data generator comprising an array of interconnections ~~for transferring~~ to transfer the address bit sequence from the address generator to a data input of the memory.

6. (Currently Amended) ~~A~~ The semiconductor integrated circuit according to claim ~~1,~~ 9 wherein the pattern is a checkerboard pattern in the memory.

7. (Currently Amended) ~~A~~ The semiconductor integrated circuit according to claim ~~1,~~ 9 wherein the pattern is so arranged that the ~~RAM~~ memory may be modeled as a simple combinational circuit.

8. (Currently Amended) ~~A~~ The semiconductor integrated circuit according to claim ~~1,~~ 9 wherein the testing arrangement comprises a wrapper circuit ~~for selectively preloading~~ to selectively preload the memory, or ~~for connecting~~ to connect the memory to other components in the integrated circuit.

9. (Currently Amended) ~~A semiconductor integrated circuit according to claim 1~~ A semiconductor integrated circuit comprising a plurality of combinational logic components, a memory and a testing arrangement to configure the memory prior to testing the combinational logic components using one or more scan chains, the testing arrangement comprising:

a data generator internal to the integrated circuit to generate a selected bit pattern to write to the memory;

a switching arrangement to selectively switch the memory input to receive data from the combinational logic components or from the data generator; wherein the switching arrangement and data generator are arranged for the data generator to input the selected bit pattern to the memory prior to testing the combinational logic components of the integrated circuit; and

a testing circuit to test the combinational logic components, using a test pattern, after the data generator has input the selected bit pattern to the memory, wherein the testing arrangement comprises a wrapper circuit and includes a control ~~for selectively controlling~~ to selectively control the memory to behave as a ROM after writing the selected bit pattern to the memory, and while testing the integrated circuit using the test pattern.

10. (Currently Amended) A semiconductor circuit, comprising:

a memory array;

a plurality of logic elements selectively coupled to the memory array;

a data generator selectively coupled to the memory array ~~for generating~~ to generate a selected bit pattern ~~for writing~~ to write to the memory array;

a switching circuit ~~for selectively coupling~~ to selectively couple the logic elements or the data generator to input data into the memory array at a selected time under control of a control circuit; and

a logic testing circuit coupled to the logic elements configured to test the operation of the logic elements based on ~~the selected~~a test bit pattern that is input to the logic elements and that is different from the selected bit pattern present in the memory array.

11. (Currently Amended) The semiconductor circuit according to claim 10 wherein said switching circuit includes a multiplexer having one input coupled to the logic elements and another input coupled to the data generator and a control input coupled to the control circuitry to selectively connect the memory array to the logic elements or to the data generator.

12. (Currently Amended) The semiconductor circuit according to claim 10 wherein said data generator creates ~~a~~ the selected bit pattern for loading into the memory array prior to testing of the semiconductor circuit.

13. (Currently Amended) The semiconductor circuit according to claim 12 wherein the bit pattern which is selected for a given address in the memory array is a function of ~~the~~ an address bit sequence.

14. (Currently Amended) The semiconductor circuit according to claim 10 in which the time selected for coupling the data generator to the memory array is prior to testing of

the semiconductor circuit so that ~~a~~ the selected bit pattern is input by the data generator into the semiconductor circuit prior to testing.

15. (Currently Amended) The semiconductor circuit according to claim 13 further comprising:

an address generator ~~for generating~~ to generate addresses of the memory array to which the bit pattern is to be written and the data generator includes an array of inner connections ~~for transferring~~ to transfer the address bit sequence from the address generator to a data input of the memory array.

16. (Currently Amended) The semiconductor circuit according to claim 13 in which the bit pattern which is written to the memory array is selected based on ~~the~~ a type of memory to which the selected bit pattern is to be written.

17. (Currently Amended) The ~~integrated~~ semiconductor circuit according to claim 16 wherein the memory is a RAM.

18. (Original) The semiconductor circuit according to claim 16 wherein the memory is a CAM.

19. (Currently Amended) The semiconductor circuit according to claim 10 wherein the control circuit selects a time ~~for controlling~~ to control input provided to the memory array and further including a memory array enable circuit to enable the input of data to the memory array prior to testing and to disable data input into the memory array after ~~a~~ the selected bit pattern has been written to the memory array and during testing of the semiconductor circuit such that during testing, the memory array behaves as a ROM.

20. (Currently Amended) A method of testing logic in ~~the~~ a same integrated circuit as a semiconductor integrated memory circuit, the method comprising:

switching a memory input with a multiplexer to receive address, data, and control signals, in a first state, from an external interface or, in a second state, from an internal address counter, an internal data generator and an internal test control circuit;

during the second state:

generating an address with the internal address counter for determining ~~the~~ an address at which data will be written;

coupling an output of the internal address counter with an input of the internal data generator;

generating a ~~selected~~ first bit pattern with the internal data generator based upon ~~the~~ a value of the internal address counter;

writing the ~~selected~~ first bit pattern into a memory at the ~~location~~ address specified by the internal address counter; and

inputting ~~selected data~~a second bit pattern, different from the first bit pattern, into the logic to be tested after writing the first bit pattern into the memory; and

~~transferring signals from the logic to be tested to the memory and from the memory to the logic to~~ testing the logic using the second bit pattern, in a manner that an output of the memory is predictable based on the first bit pattern written therein and is independent of the second bit pattern.

21. (Currently Amended) The method of testing logic in the same integrated circuit as the semiconductor integrated memory circuit according to claim 20, wherein the ~~selected~~ first bit pattern to be generated ~~consists of~~comprises a checkerboard pattern.

22. (Currently Amended) The method of testing logic in the same integrated circuit as the semiconductor integrated memory circuit according to claim 21, wherein the memory ~~to be tested consists of~~ comprises a Content Addressable Memory.

23. (Currently Amended) The method of claim 20 wherein testing the logic using the second bit pattern, in a manner that the output of the memory is predictable based on the first bit pattern written therein ~~further including:~~includes placing the memory in a state that simulates a combinatorial logic function.

24. (Currently Amended) A method of testing logic elements that are in ~~the~~ a same integrated circuit as a memory array, the method comprising:

inputting to the memory array a ~~selected~~ first pattern of data bits, the first pattern being selected to configure the memory array to operate as a combinatorial logic circuit ~~for the input of signals and the output of signals based on the input~~;

setting the integrated circuit in logic test mode for testing logic that is outside of the memory array;

inputting ~~signals from the logic into~~to the logic a second pattern of data bits, different from the first pattern of data bits in the memory array, as part of testing the logic after the first pattern of data bits is input to the memory array;

receiving output from the memory array ~~as part of~~ during the testing of the logic, the output of the memory array being predictable based on the first bit pattern and being independent of the second bit pattern input to ~~acting as a portion of~~ the logic ~~circuit during~~for the testing of the logic ~~elements of the integrated circuit~~.

25. (Currently Amended) The method according to claim 24 further including:

sending signals via a scan chain between respective logic elements of the logic being tested.